What is claimed is:

1. An information processing device for, when an input address causes a cache miss, storing and reading the input address including first and second fields on a FIFO basis to provide the input address to a main memory control circuit, the device comprising:

a first register file including a plurality of first registers for storing, in each first register, a first address consisting of the first and second fields, a valid flag indicating whether the first address is valid or invalid, and wait state information;

a second register file including a plurality of second registers, corresponding to the respective plurality of first registers, for storing, in each second register, a second address consisting of the second field, and a valid flag indicating whether the second address is valid or invalid;

a comparison circuit for comparing a value of the first field of the input address and a value of the first field of each of the plurality of first registers; and

a control circuit for:

allowing the input address to be stored in one of the first registers whose valid flag indicates an invalid state, and changing this valid flag to indicate a valid state, or, if a comparison result by the comparison circuit between one

of the first registers whose valid flag indicates a valid state and the input address indicates a matching, then allowing the second field of the input address to be stored in corresponding one of the second registers whose valid flag indicates an invalid state, and changing this valid flag to indicate a valid state; and

selectively allowing contents of one of the first registers whose valid flag indicates a valid state to be read; if the valid flag of corresponding one of the second registers indicates an invalid state, then changing this valid flag to indicate an invalid state, or else, allowing a value of the second field of this one of the second registers to be shifted to the second field of the corresponding one of the first registers, and changing the valid flag of this one of the second registers to indicate an invalid state.

2. The information processing device according to claim 1, further comprising:

a selective transmission circuit for, in a write operation, allowing the input address to be transferred to selected one of the first or second registers, and, in a read operation, allowing contents of the second field of selected one of the second registers to be shifted toward corresponding one of the first registers.

3. The information processing device according to claim 2, wherein the control circuit includes a write pointer and the control circuit:

(1) if a valid flag of one of the first registers pointed to by the write pointer indicates an invalid state, then controls the selective transmission circuit to allow the input address to be stored in the one of the first registers pointed to by the write pointer, and changes this valid flag to indicate a valid state;

(2) or else,

(a) if a comparison result by the comparison circuit between the one of the first registers pointed to by the write pointer and the input address indicates a matching, then controls the selective transmission circuit to allow the input address to be stored in one of the second registers pointed to by the write pointer, changes a valid flag of this one of the second registers to indicate a valid state, and allows the write pointer to be incremented,

(b) or else, allows the write pointer to be incremented, controls the selective transmission circuit to allow the input address to be stored in the one of the first registers pointed to by the write pointer, and changes the valid flag of this one of the first registers to indicate a valid state.

4. The information processing device according to claim 2, wherein the control circuit includes a read pointer and the control circuit:

(3) allows contents of one of the first registers pointed to by the read pointer to be read; and

(4) (c) if a valid flag of one of the second registers pointed to by the read pointer indicates an invalid state, then changes a valid flag of one of the first registers pointed to by the read pointer to indicate an invalid state, and allows the read pointer to be incremented,

(d) or else, controls the selective transmission circuit to allow a value of the second field of this one of the second registers to be shifted to the corresponding one of the first registers so as to be written to the second field of this one of the first registers, and changes the valid flag of this one of the second registers to indicate an invalid state.

5. The information processing device according to claim 3, wherein the control circuit includes a read pointer and the control circuit:

(3) allows contents of one of the first registers pointed to by the read pointer to be read; and

(4) (c) if a valid flag of one of the second registers

pointed to by the read pointer indicates an invalid state, then changes a valid flag of one of the first registers pointed to by the read pointer to indicate an invalid state, and allows the read pointer to be incremented,

(d) or else, controls the selective transmission circuit to allow a value of the second field of this one of the second registers to be shifted to the corresponding one of the first registers so as to be written to the second field of this one of the first registers, and changes the valid flag of this one of the second registers to indicate an invalid state.

6. The information processing device according to claim 1, wherein a plurality of the second register files are provided, each second register file having a plurality of registers in a column, and the plurality of the second register files are connected in cascade in regard to each register row of the plurality of the second register files, and the device further comprises:

a selective transmission circuit for, in a write operation, allowing the input address to be transferred to selected one of the registers in the first or second register files, and, in a read operation, allowing contents of the second field of selected registers of one row of the second register files to be shifted toward corresponding one

of the first registers.

7. The information processing device according to claim 6, wherein the control circuit includes a write pointer and the control circuit:

(1) if a valid flag of one of the first registers pointed to by the write pointer indicates an invalid state, then controls the selective transmission circuit to allow the input address to be stored in the one of the first registers pointed to by the write pointer, and changes this valid flag to indicate a valid state;

(2) or else,

(a) if a comparison result by the comparison circuit between the one of the first registers pointed to by the write pointer and the input address indicates a matching, then

controls the selective transmission circuit to allow the input address to be stored in one of the second registers whose valid flag indicates an invalid state and whose neighboring one of the second registers has a valid flag indicating a valid state, changes the valid flag of this one of the second registers to indicate a valid state, and allows the write pointer to be incremented,

(b) or else, allows the write pointer to be incremented, controls the selective transmission circuit to

allow the input address to be stored in the one of the first registers pointed to by the write pointer, and changes the valid flag of this one of the first registers to indicate a valid state.

8. The information processing device according to claim 6, wherein the control circuit includes a read pointer and the control circuit:

(3) allows contents of one of the first registers pointed to by the read pointer to be read; and

(4) (c) if all valid flags of second registers of the second register files in a row pointed to by the read pointer indicate an invalid state, then changes a valid flag of this one of the first registers pointed to by the read pointer to indicate an invalid state, and allows the read pointer to be incremented,

(d) or else, controls the selective transmission circuit to allow contents of the second fields of the second registers in the row to be shifted toward the first register file, and changes a valid flag having a valid state at an upstream end side, with respect to the shift direction, to indicate an invalid state.

9. The information processing device according to claim 7, wherein the control circuit includes a read pointer

and the control circuit:

(3) allows contents of one of the first registers pointed to by the read pointer to be read; and

(4) (c) if all valid flags of second registers of the second register files in a row pointed to by the read pointer indicate an invalid state, then changes a valid flag of this one of the first registers pointed to by the read pointer to indicate an invalid state, and allows the read pointer to be incremented,

(d) or else, controls the selective transmission circuit to allow contents of the second fields of the second registers in the row to be shifted toward the first register file, and changes a valid flag having a valid state at an upstream end side, with respect to the shift direction, to indicate an invalid state.

10. The information processing device according to claim 1, wherein the first and second fields are defined in relation to a cache memory, the first field consists of a tag field and an entry field, and the second field is an offset field which is lower order than the entry field.

11. The information processing device according to claim 1, wherein the first and second fields are defined in relation to a cache memory, the first field is an entry

field, and the second field consists of a tag field of higher order than the entry field and an offset field of lower order than the entry field.

12. The information processing device according to claim 1, wherein the first and second fields are defined in relation to a cache memory, the first field is a tag field, and the second field consists of an entry field of lower order than the tag field and an offset field of lower order than the entry field.